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UNITED STATES PATENT APPLICATION

of

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for

APPARATUS AND METHOD FOR DEMODULATING A RADIO DATA SYSTEM (RDS) SIGNAL

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BACKGROUND OF THE INVENTION

The present invention relates to Radio Data System (RDS) signals broadcast with VHF radio transmissions, and in particular, to a method and circuitry for demodulating the RDS signal.

DESCRIPTION OF THE RELEVANT ART

The Radio Data System, or RDS, is a information broadcast that was introduced for use in FM radio stations which transmit stereo-multiplex signals in the VHF frequency band. The Radio Data System provides radio receivers with broadcast data about the transmitting radio station and the programs broadcast by the radio station. The radio receivers typically reproduce this data on an optical display such as a liquid-crystal display screen.

The RDS broadcast data may include program identification (PI) which indicates the program being received or the name of the station/transmitter tuned in; program type identification (PTY) which indicates the type of program such as music, news, etc.; traffic announcements (TA); and/or radio text (RT) which contains program-accompanying information such as the music title, performer, program changes, and the like.

The Radio Data System is used principally in car radios. For example, when the reception of the transmitter currently tuned in deteriorates, RDS-capable car radios automatically switch over to a better, or best receivable, transmitter broadcasting the same program. The information required to do this is includes the noted program identification (PI) information along with a list of alternative frequencies (AF) which are being broadcast by RDS-capable radio stations. The Radio Data System

also offers advantages to the listener of home FM receivers as well. For example, the home listener can benefit from the noted program type identification (PTY) and radio text (RT) which information.

As noted, the VHF signal transmitted by FM radio stations is referred to as a stereo-multiplex signal. A stereo-multiplex signal includes the following components: an audio center (mono) signal at up to 15 kHz; a stereo pilot tone at 19 kHz; a stereo signal between 23 kHz and 53 kHz, and an ARI (*Autofahrer-Rundfunk-Information-System* (German), referred to as Motorist Information System in the United States) signal.

The ARI signal component is a narrowband amplitude-modulated signal with a carrier frequency of 57 kHz. The RDS signal is a binary signal that consists of a continuous binary data stream with a bit rate of 1.1875 Kbits/s. The RDS signal, which has a greater bandwidth than the ARI signal, is superimposed on the ARI signal. The RDS signal is generated from the RDS data stream by double-sideband modulation with carrier suppression. In addition, the suppressed RDS carrier is phase-shifted by 90° relative to the ARI carrier at 57 kHz. Because of this quadrature modulation, interference with the ARI signal by the RDS signal is essentially suppressed. In an RDS-capable radio transmitter, the carrier is frequency-modulated by the stereo-multiplex signal formed in the above-described manner and broadcast. The prevent the RDS signal from interfering with the other component signals such as the audio center signal, the stereo signal and the stereo pilot tone, while achieving a high data rate, the frequency spectrum of the RDS signal is typically restricted to ± 2.4 kHz.

On the receiver side, the received frequency-modulated carrier is demodulated to obtain the stereo-multiplex signal from which the RDS signal as well as the audio signals are obtained. One challenge for mobile FM receivers such as those installed in automobiles is that it can take considerable time before the tuner is synchronized to the 57 kHz carrier of the RDS signal due to

constantly changing and often unsatisfactory reception conditions. There is a need, therefore, for a technique for demodulating the RDS signal such that the fastest possible synchronization with the carrier of the RDS signal is achieved.

SUMMARY OF THE INVENTION

Briefly, according to an aspect of the invention, a phase-locked loop circuit for demodulating a Radio Data System (RDS) signal superimposed on an ARI signal component of a stereo-multiplex signal is disclosed. The circuit comprises: an oscillator that generates an in-phase component signal and a quadrature component signal of the carrier of the RDS signal; a first circuit branch comprising a first multiplier having a first input at which a sampled stereo-multiplex signal is received and a second input at which the in-phase component signal is received, a first low-pass filter having an input connected to an output of the first multiplier, a first divider having an input connected to an output of the first low-pass filter, and a first high-pass filter having an input connected to an output of the first divider; a second circuit branch comprising a second multiplier having a first input at which the sampled stereo-multiplex signal is received , and a second input at which the quadrature component signal is received, a second low-pass filter having an input connected to an output of the second multiplier, a second divider having an input connected to an output of the second low-pass filter, and a second high-pass filter having an input connected to an output of the second divider; a feedback branch comprising an arithmetic unit having first and second inputs connected to outputs of the first and second high-pass filters, respectively, a clock input at which an RDS bit clock signal is received, and an output at which the arithmetic unit generates an error signal; a filter having an input at which it receives the error signal, and an output at which it generates a filtered error signal; a control unit having an input connected to the filter output, and an output connected to a control input

of the oscillator at which the control unit generates a control signal in response to the error signal; a clock generator having a first control input connected to the output of the first high-pass filter, a second control input connected to an output of the oscillator, and an output at which the clock generator generates the RDS bit clock signal; and an RDS decoder having a first input connected to the output of the first high-pass filter, a clock input at which the RDS bit clock signal is received, and an output from which RDS data is retrievable.

In another aspect of the invention, a method for demodulating a Radio Data System (RDS) signal superimposed on an ARI signal component of a stereo-multiplex signal. The method comprises the steps of: generating an in-phase component signal and a quadrature component signal of the carrier of the RDS signal; multiplying a sampled stereo-multiplex signal by the in-phase component to generate a first product signal; low-pass filtering the first product signal to generate a first low-pass filtered signal; dividing a sampling rate of the first low-pass-filtered signal by a first presettable division factor to generate a decimated, filtered first product signal; high-pass filtering the decimated, filtered first product signal to generate a first high-pass-filtered signal; decoding the first high-pass filtered signal to generate RDS data; multiplying the sampled stereo-multiplex signal by the quadrature component of the digital oscillator to generate a second product signal; low-pass filtering the second product signal to generate a second low-pass filtered signal; dividing a sampling rate of the second low-pass-filtered signal by a second presettable division factor to generate a decimated, filtered second product signal; high-pass filtering the decimated, filtered second product signal to generate a second high-pass-filtered signal; calculating an error signal representing a phase difference between the carrier of the RDS signal and the output signal of the oscillator based on the first and second high-pass-filtered signals and an RDS clock signal, wherein the error signal represents a phase position between the carrier of the RDS signal and the output signal of the

oscillator; and generating a correction signal for controlling the oscillator based on the error signal.

In a still further aspect of the invention, a phase-locked loop circuit for demodulating a Radio Data System (RDS) signal superimposed on an ARI signal component of a stereo-multiplex signal, the circuit comprising: means for generating an in-phase component signal and a quadrature component signal of an RDS carrier signal in response to an oscillator control signal; means for generating a first product signal of a sampled stereo-multiplex signal and the in-phase component signal; means for generating a second product signal of a sampled stereo-multiplex signal and the quadrature component signal; means for controlling the oscillator based on the phase relationship between the RDS carrier signal and the signals generated by the oscillator; and means for generating RDS data based on the first high-pass filter.

These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

The FIGURE is a schematic block diagram of one embodiment of a phase-locked loop (PLL) circuit.

DETAILED DESCRIPTION OF THE INVENTION

The FIGURE is a schematic block diagram of one embodiment of a phase-locked loop 100 (PLL). The PLL circuit 100 rapidly demodulates the RDS signal superimposed on the ARI signal of a received stereo-multiplex signal.

PLL circuit 100 receives a sampled stereo-multiplex signal 102 and processes the received signal 102 through two branches. The sampling frequency for sampling stereo-multiplex signal 102 is selected such that the spectrum of the RDS signal is represented completely and correctly in the region of the 57 kHz carrier. Preferably, the sampling frequency for sampling stereo-multiplex signal 102 is greater than 120 kHz. The sampled stereo-multiplex signal 102 is applied to the first input of a multiplier 104 of the first branch and a multiplier 106 of the second branch. The in-phase component 108 of a digital oscillator 110 is applied to the second input of multiplier 104, while a quadrature component 112 of digital oscillator 110 is applied to the second input of multiplier 106.

The output of multiplier 104 is connected to the input of a low-pass filter 114. The output of low-pass filter 114 is connected to the input of a divider 116. Low-pass filter 114 generates a low-pass-filtered signal. The sampling rate of the low-pass filter is divided by a division factor described below in divider 116. The resulting low-pass filter is decimated in the sampling rate. The output of divider 116 is connected to the input of a high-pass filter 118, the output of which represents the end of the first branch, and is connected to the input of an RDS decoder 120 and to the first input of an

arithmetic unit 122. The low-pass-filtered signal is filtered by high-pass filter 118 and decoded in RDS decoder 120.

In the second branch, sampled stereo-multiplex signal 102 is multiplied by quadrature component 112 of the digital oscillator 110 in multiplier 106. The output of multiplier 106 is connected to the input of a low-pass filter 124. Low-pass filter 124 filters the resulting product signal generated by multiplier 106. The output of low-pass filter 124 is connected to the input of a divider 126. Divider 126 divides the sampling rate of the resulting low-pass-filtered signal. The output of divider 126 is connected to the input of a high-pass filter 128. High-pass filter 128 filters the decimated low-pass-filtered signal generated by divider 126. The output of high-pass filter 128 represents the end of the second branch and is connected to the second input of arithmetic unit 122. The output of arithmetic unit 122 is connected, via a filter 130, preferably a loop filter, to a control unit 132. Control unit 132 has an output connected to the control input of digital oscillator 110.

An RDS bit clock signal 134 is generated by a clock generator 138 with a clock output that is connected to the clock input of arithmetic unit 122 and the clock input of RDS decoder 120. The output of high-pass filter 118 is connected to the first input of clock generator 130 while the output of digital oscillator 110 to the second input of clock generator 130. Arithmetic unit 122 as well as RDS decoder 120 are clocked by clock generator 138.

Using the high-pass-filtered signal of the first and second branches as well as RDS bit clock 134, arithmetic unit 122 calculates an error signal 136 describing the phase deviation between the carrier of the RDS signal and the output signal of oscillator 110. Control unit 132 generates a correction signal 140 based on error signal 136 for controlling digital oscillator 110.

Thus, sampled stereo-multiplex signal 102 is multiplied in a first branch in multiplier 104 by in-phase component 108 of digital oscillator 110, then filtered in low-pass filter 114, its sampling

rate is divided in the following divider 116, and finally, stereo-multiplex signal 102 is filtered in high-pass filter 118. In parallel, the sampled stereo-multiplex signal 102 is multiplied in multiplier 106 by quadrature component 112 of digital oscillator 110, then filtered in low-pass filter 124; in the following divider 126, its sampling rate is divided and is finally high-pass-filtered in high-pass filter 128.

The first and second division factors for decimating the sampling rate of the two low-pass-filtered signals are preferably selected such that the RDS signal is correctly represented in the baseband. In one embodiment, the first and second division factors are preferably 16 although other division factors can be implemented. The two high-pass filters 118 and 128 function to suppress low-frequency signal components which may be caused by an ARI signal contained in stereo-multiplex signal 102. In one embodiment, the clock frequency of the RDS signal and the frequency of digital oscillator 110 are each 57 kHz.

Since calculation of error signal 136 in arithmetic unit 122 is coupled to RDS bit clock 134, error signal 136 is calculated only at those times when in-phase component 108 is at a maximum. This occurs after a quarter-bit clock period and a three-quarter-bit clock period. This measure ensures that a situation is avoided in which error signal 136 is calculated by arithmetic unit 122 at a point in time when in-phase component 108 shows a zero crossing.

As long as the phase-locked loop is not yet synchronized with the carrier of the RDS signal, clock generator 138 runs free. To preclude calculation of an error signal in arithmetic unit 122 in the event of a zero crossing of in-phase component 108 of digital oscillator 110, the amplitude of the in-phase component is checked. During this initialization phase of carrier synchronization, the calculation cycle for the error signal may be shifted by a quarter clock period if a zero crossing is detected in in-phase component 108. This measure ensures very rapid and reliable synchronization

with the carrier of the RDS signal. A further advantage of the present invention is that it the above operations can be implemented as software.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is: